REMARKS

Claims 1, 4-5, 7-9, 12, 15, 17, and 19 are currently amended and claims 24-30 are added. Claims 1-30 are now pending. Applicant contends that the amendments contained herein and the added claims are supported by the Specification as filed and thus do not constitute new matter.

Rejections Under 35 U.S.C. § 102

Claims 1-23 were rejected under 35 U.S.C. § 102 (b) as being anticipated by Schumann et al. (U.S. Patent 5,732,017). Claims 1-23 were rejected under 35 U.S.C. § 102 (b) as being anticipated by Pashley et al. (U.S. Patent 6,418,506). Applicant respectfully submits that Pashley et al. falls under 35 U.S.C. § 102 (e) rather than 35 U.S.C. § 102 (b), and Applicant reserves the right to swear behind Pashley et al. Claims 1-23 were rejected under 35 U.S.C. § 102 (b) as being anticipated by Akaogi et al. (U.S. Patent 6,240,040). Applicant respectfully submits that Akaogi et al. falls under 35 U.S.C. § 102 (e) rather than 35 U.S.C. § 102 (b), and Applicant reserves the right to swear behind Akaogi et al. Applicant respectfully traverses these rejections.

Each of claims 1, 7, and 9, as currently amended, includes read/write circuitry that writes first data to a first one of a plurality of addressable banks of an array of non-volatile memory cells and simultaneously reads second data from two or more remaining banks of the plurality of addressable banks of the array of non-volatile memory cells.

Applicant carefully reviewed Schumann et al., Pashley et al., and Akaogi et al. and found no indication of read/write circuitry that writes first data to a first one of a plurality of addressable banks of an array of non-volatile memory cells and simultaneously reads second data from two or more remaining banks of the plurality of addressable banks of the array of non-volatile memory cells, as in each of claims 1, 7, and 9. This means that the read/write circuitry of each of claims 1, 7, and 9 writes to and simultaneously reads from the *same* array of non-volatile memory cells. In contrast, Schumann et al. concurrently reads flash memory 11 during a write cycle period of a *separate* E^2PROM array 13 (Figure 1 and column 6, lines 43-44). In Schumann et al., an E^2PROM read cannot be performed during any of the write cycles (column 7, lines 27-

28). Pashley et al. reads from a RAM array during at least a portion of a period of time in which data is written to a *separate* flash array (Column 5, lines 11-14). Alternatively, Pashley et al. writes to the RAM array during at least a portion of a period of time in which data is read from the flash array (Column 5, lines 14-18).

In each of claims 1, 7, and 9, read/write circuitry writes first data to a first one of the plurality of addressable banks and simultaneously reads second data from *two or more remaining banks* of the plurality of addressable banks. However, in Akaogi et al., for the duration of a read operation at one bank of N banks, a write operation can *only* be performed on any *one* of the other N-1 banks, and for the duration of a write operation at one bank of the N banks, a read operation can *only* be performed on any *one* of the other N-1 banks (column 2, lines 56-60).

In view of the above, neither Schumann et al., Pashley et al., nor Akaogi et al. include each and every element of each of claims 1, 7, and 9. Therefore, each of claims 1, 7, and 9 should be allowed.

Claims 2-6 depend directly from claim 1 and thus include patentable limitations of claim 1. Claim 8 depends directly from claim 7 and thus includes patentable limitations of claim 7. Claim 10 depends directly from claim 9 and thus includes patentable limitations of claim 9. Therefore, claims 2-6, claim 8, and claim 10 should be allowed.

Claim 11 includes read/write circuitry that writes first data provided by a first processor to a first one of a plurality of addressable banks and simultaneously reads second data from a second one of the plurality of addressable banks and provides the second data to a second processor. There is no indication of this in Schumann et al., Pashley et al., or Akaogi et al. Therefore, neither Schumann et al., Pashley et al., nor Akaogi et al. include each and every element of claim 11, and claim 11 should be allowed.

Each of claims 12 and 17, as currently amended, includes writing first data to a first bank location in a memory array, substantially simultaneously reading second data

from a second bank location in the memory array, and substantially simultaneously reading third data from a third bank location in the memory array.

Applicant carefully reviewed Schumann et al., Pashley et al., and Akaogi et al. and found no indication of writing first data to a first bank location in a memory array, substantially simultaneously reading second data from a second bank location in the memory array, and substantially simultaneously reading third data from a third bank location in the memory array, as in each of claims 12 and 17. This means that first data is written to and substantially simultaneously second and third data are read from the *same* array of non-volatile memory cells. In contrast, Schumann et al. concurrently reads flash memory 11 during a write cycle period of a *separate* E^2PROM array 13 (Figure 1 and column 6, lines 43-44). In Schumann et al., an E^2PROM read cannot be performed during any of the write cycles (column 7, lines 27-28). Pashley et al. reads from a RAM array during at least a portion of a period of time in which data is written to a *separate* flash array (Column 5, lines 11-14). Alternatively, Pashley et al. writes to the RAM array during at least a portion of a period of time in which data is read from the flash array (Column 5, lines 14-18).

In each of claims 12 and 17, first data is written to a first bank location of a memory array, second data is substantially simultaneously read from a second bank location of the memory array, and third data is substantially simultaneously read from a third bank location of the memory array. However, in Akaogi et al., for the duration of a read operation at one bank of N banks, a write operation can *only* be performed on any *one* of the other N-1 banks, and for the duration of a write operation at one bank of the N banks, a read operation can *only* be performed on any *one* of the other N-1 banks (column 2, lines 56-60).

In view of the above, neither Schumann et al., Pashley et al., nor Akaogi et al. include each and every element of each of claims 12 and 17. Therefore, each of claims 12 and 17 should be allowed.

Claims 13-16 depend directly from claim 12 and thus include patentable limitations of claim 12. Claims 18-20 depend directly or indirectly from claim 17 and

thus include patentable limitations of claim 17. Therefore, claims 13-16 and claims 18-20 should be allowed.

Claim 21 includes receiving first data from a first external processor coupled to the memory, writing the first data to a first location in a memory array of the non-volatile memory device, substantially simultaneously reading second data from a second location in the memory array of the non-volatile memory device, and outputting the second data to a second external processor coupled to the memory device. There is no indication in Schumann et al., Pashley et al., or Akaogi et al. of writing first data received from a first processor to a first one of a plurality of addressable banks and simultaneously reading second data from a second one of the plurality of addressable banks and providing the second data to a second processor. Therefore, neither Schumann et al., Pashley et al., nor Akaogi et al. include each and every element of claim 21, and claim 21 should be allowed.

Claims 22-23 depend directly or indirectly from claim 21 and thus include patentable limitations of claim 21. Therefore, claims 22-23 should be allowed.

Double Patenting Rejection

The Examiner provisionally rejected claims 1-23 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-27 of co-pending U. S. Patent Application No. 09/627,770 (the '770 application). Applicant respectfully traverses this rejection.

Claims 1-23 of the present application include writing first data to one bank of a plurality of addressable banks of an array of non-volatile memory cells and simultaneously reading second data from another bank of the plurality of addressable banks of the array of non-volatile memory cells. In contrast, claims 1-27 of the '770 application include writing to an array bank while reading data from a buffer connected to the array bank, where the data has been copied from the array bank to the buffer. Therefore, claims 1-23 of the present application are patentably distinct from claims 1-27 of the '770 application because claims 1-27 of the '770 application require limitations not included in claims 1-23 of the present application. Therefore, the rejection of claims 1-23

under the judicially created doctrine of obviousness-type double patenting should be removed, and claims 1-23 should be allowed.

Added Claims

Claims 24-30 are added. Claim 24 includes read/write circuitry that writes first data to a first one of a plurality of addressable banks and simultaneously reads second data from a second one of the plurality of addressable banks, wherein the read/write circuitry receives the first data from a first external processor and provides the second data to a second external processor. There is no indication of this in Schumann et al., Pashley et al., or Akaogi et al. Therefore, neither Schumann et al., Pashley et al., nor Akaogi et al. include each and every element of claim 24, and claim 24 should be allowed.

Claims 25-28 depend directly from claim 24 and thus include patentable limitations of claim 24. Therefore, claims 25-28 should be allowed.

Claim 29 includes providing first data to a non-volatile memory from a first external processor, writing the first data to a first bank location in a memory array of the non-volatile memory, substantially simultaneously reading second data from a second bank location in the memory array of the non-volatile memory, and outputting the second data to a second external processor. There is no indication in Schumann et al., Pashley et al., or Akaogi et al. of writing first data from a first external processor to a first one of a plurality of addressable banks and substantially simultaneously reading second data from a second one of the plurality of addressable banks and outputting the second data to a second external processor. Therefore, neither Schumann et al., Pashley et al., nor Akaogi et al. include each and every element of claim 29, and claim 29 should be allowed.

Claim 30 depends directly from claim 29 and thus includes patentable limitations of claim 29. Therefore, claim 30 should be allowed.

Applicant respectfully requests admission and allowance of claims 24-30.

CONCLUSION

Claims 1, 4-5, 7-9, 12, 15, 17, and 19 are currently amended and claims 24-30 are added. Claims 1-30 are now pending. In view of the above remarks, Applicant respectfully submits that the claims are in condition for allowance and requests reconsideration of the application and allowance of the claims.

The Examiner is invited to contact Applicant's representative at 612 312-2208 if there are any questions regarding this response or if prosecution of this application may be assisted thereby.

Respectfully submitted,

Date: 11-10-2003

Tod A. Myrum
Reg. No. 42,922

Attorneys for Applicant
Leffert Jay & Polglaze, P.A.
P.O. Box 581009
Minneapolis, MN 55458-1009
telephone: (612) 312-2200
facsimile: (612) 312-2250